REMARKS

This Amendment is in response to the Office Action dated December 22, 2004. In the Office Action, claims 1-20 were rejected under 35 USC §102. By this Amendment, claim 15 is canceled and claim 16-20 are amended. Currently pending claims 1-14 and 16-20 are believed allowable, with claims 1, 7, 16 and 17 being independent claims.

AMENDMENTS TO THE DRAWINGS:

Figs. 6, 10-13 and 15-20 were objected to as designating that which is the invention as "Prior Art". The "Prior Art" captions are removed from Figs. 10-13 and 15-20 by this Amendment.

CLAIM REJECTIONS UNDER 35 USC §102:

Claims 1, 2, 4, 5, 7, 8, 10, 11, 13-18 and 20 were rejected under 35 USC §102 as being anticipated by U.S. Patent No. 5,107,503 to Riggle et al. ("Riggle"). To anticipate a claim under 35 USC §102, a reference must teach every element of the claim. MPEP 2131.

Claim 1:

Claim 1 recites a plurality of multipliers, wherein the multipliers include, "an input side XOR calculator, an AND calculator, and an output side XOR calculator, and wherein said multipliers share said input side XOR calculator." It is respectfully submitted that Riggle does not teach or suggest such claim limitations.

Turning to the specific citations of Riggle in the Office Action (Office Action, page 3), discussion is made in the Abstract of Riggle about using first and second Galios Field multipliers to iteratively determine syndromes. Nevertheless, there is no mention in the Abstract of either an input side XOR calculator, an AND calculator, or an output side XOR calculator as recited in claim 1 of the present Application. Specifically, the Abstract states,

> A pipelined error correction circuit iteratively determines syndromes, error locator and evaluator equations, and error locations and associated error values for received Reed-Solomon code words. The circuit includes a plurality of Galois Field multiplying circuits which use a minimum number of circiut elements to generate first and second products. Each Galois Field multiplying circuit includes a first GF multiplier which multiplies one of two input signals in each of two time intervals by a first value to produce a first product. The circuit includes a second GF multiplier which further multiplies one of the first products by a second value to generate a second product. The

> first and second products are then applied to the first GF multiplier as next input signals. The multiplying circuit minimizes the elements required to generate two products by using a first, relatively complex multiplier for both the first and second products and then a second relatively simple multiplier to generate the second product. This simplifies the multiplying circuit which would otherwise require two relatively complex multipliers. The error correction circuit determines, for each received code word, an error locator equation by iteratively updating a preliminary error locator equation. The circuit determines for a given iteration whether or not to update the preliminary error locator equation by comparing a particular variable with zero. Riggle, Abstract, lines 1-27.

Column 8, lines 4 to 5 of Riggle state, ". . . the Galois Field multiplier circuits, defined mathematically below, can be reduced by a factor of 2, that is . . ." Riggle, col. 8, lines 4-5. It is respectfully submitted that this text does not teach or suggest an input side XOR calculator, an AND calculator, or an output side XOR calculator as recited in claim 1 of the present Application.

Column 9, lines 6 to 29 of Riggle describe the operations of the Galois Field multiplication function. This portion of the patent discloses a conventional AND-XOR structure for realizing the multiplication function. Riggle, col. 9, lines 23-26. There is no mention, however, of the XOR-AND-XOR multiplier structure as recited in claim 1 of the present Application.

Likewise, at column 23, line 66 to column 24, line 24 of Riggle, there is no mention of the XOR-AND-XOR multiplier structure as recited in claim 1 of the present Application. Specifically, the cited passage states,

> the multiplier means comprising:
> a. a logical AND circuit responsive to a feedback signal and an input signal for providing a first output signal;
> b. a GF multiplier responsive to the first output signal for GF multiplying the first output signal by a predetermined value at a predetermined time to obtain a second output signal;
> c. a storage register for storing the second output signal; and
> d. a GF adder for adding the stored second output signal to a data signal and providing the sum as the input signal to the logical AND circuit. Riggle, col. 23, line 66 - col. 24, line 24.

For at least these reasons, claim 1 is not believed to be anticipated by Riggle. Moreover, it is respectfully submitted that claim 1 is allowable and indication of such allowance is earnestly requested.

Claims 2-6:

Claims 2-6 are dependent on and further limit claim 1. Since claim 1 is believed allowable for the above reasons, claims 2-6 are also believed allowable for at least the same reasons as claim 1.

Claim 7:

Claim 7 recites, in part, "a plurality of multipliers, each of which includes an adder connected between an AND calculator and an output side XOR calculator." It is respectfully submitted that Riggle does not teach or suggest such claim limitations.

Turning to the specific citations of Riggle in the Office Action, Fig. 3 illustrates a flow chart of the decoding process performed by a syndrome computer, the error locator NU(X) and error evaluator W(x) computer, and the factor NU(x), evaluate W(x), and correction vector YI computer circuits of an integrated circuit. Riggle, col. 4, lines 28-32. In this figure, there is no structural detail regarding the circuit components. Therefore, Fig. 3 does not teach or suggest the limitations of claim 7.

Fig. 4 includes circuit details for computing syndromes simultaneously. Riggle, col. 11, lines 8-10. Nevertheless, the circuit of Fig. 4 shows a conventional AND-XOR structure, rather than the XOR-Adder-AND multiplier structure as recited in claim 7 of the present Application. Riggle, col. 11, lines 19-25 and Fig. 4. Similarly, Figs. 10, 13 and 23 do not teach or suggest the XOR-Adder-AND multiplier structure as recited in claim 7 of the present Application.

Column 11, lines 8-25 of Riggle describe the circuit depicted in Fig. 4. Riggle, col. 11, lines 8-10. It is respectfully submitted that this cited portion of the Riggle patent describes a conventional AND-XOR structure for realizing the multiplication function. Riggle, col. 11, lines 19-25. There is no mention of the XOR-Adder-AND multiplier structure as recited in claim 7 of the present Application.

Column 15, lines 15-23 of Riggle describe the circuit depicted in Fig. 10, stating, "Circuit 448 of FIG. 10 includes means for calculating error evaluator polynomial W(x). As embodied herein, the means for computing the values of error evaluator polynomial W(x) comprises w registers 450, amend syndrome 54 registers 210, error locator polynomial NV registers 352, multiplier 350, and treed adder 354 which executes the procedure shown in

FIG. 3, including, specifically step 106." Riggle, col. 15, lines 15-23. It is respectfully submitted that this cited text in Riggle does not describe or suggest a XOR-Adder-AND multiplier structure as recited in claim 7 of the present Application.

Similarly, it is respectfully submitted that column 21, line 34 to column 22, line 5 of Riggle does not teach or suggest a XOR-Adder-AND multiplier structure as recited in claim 7 of the present Application.

For at least these reasons, claim 7 is not believed to be anticipated by Riggle. Moreover, it is respectfully submitted that claim 7 is allowable and indication of such allowance is earnestly requested.

Claims 8-14:

Claims 8-14 are dependent on and further limit claim 7. Since claim 7 is believed allowable for the above reasons, claims 8-14 are also believed allowable for at least the same reasons as claim 7.

Claim 16:

Claim 16 is amended herein to explicitly claim all the limitations of claim 15, which were previously incorporated by reference. Thus, the amendment to claim 16 is not made to change the scope of the claim, nor is amendment of claim 16 made to overcome the cited documents or for reasons of patentability.

Claim 16 recites a plurality of multipliers, wherein the multipliers include, "an input side XOR calculator, an AND calculator, and an output side XOR calculator, and wherein said multipliers share said input side XOR calculator." It is respectfully submitted that Riggle does not teach or suggest such claim limitations.

Turning to the specific citations of Riggle in the Office Action, in the Abstract of Riggle, discussion is made about using first and second Galios Field multipliers to iteratively determine syndromes. There is no mention in the Abstract of either an input side XOR calculator, an AND calculator, or an output side XOR calculator as recited in claim 16 of the present Application.

Column 8, lines 4 to 5 of Riggle state, ". . . the Galois Field multiplier circuits, defined mathematically below, can be reduced by a factor of 2, that is . . ." Riggle, col. 8, lines 4-5. It is respectfully submitted that this text does not teach or suggest an input side XOR

calculator, an AND calculator, or an output side XOR calculator as recited in claim 16 of the present Application.

Column 9, lines 6 to 29 of Riggle describe the operations of the Galois Field multiplication function. This portion of the patent discloses a conventional AND-XOR structure for realizing the multiplication function. Riggle, col. 9, lines 23-26. However, there is no mention of the XOR-AND-XOR multiplier structure as recited in claim 16 of the present Application.

Likewise, at column 23, line 66 to column 24, line 24 of Riggle, there is no mention of the XOR-AND-XOR multiplier structure as recited in claim 16 of the present Application. Specifically, the cited passage states,

> the multiplier means comprising:
> a. a logical AND circuit responsive to a feedback signal and an input signal for providing a first output signal;
> b. a GF multiplier responsive to the first output signal for GF multiplying the first output signal by a predetermined value at a predetermined time to obtain a second output signal;
> c. a storage register for storing the second output signal; and
> d. a GF adder for adding the stored second output signal to a data signal and providing the sum as the input signal to the logical AND circuit. Riggle, col. 23, line 66 - col. 24, line 24.

For at least these reasons, claim 16 is not believed to be anticipated by Riggle. Moreover, it is respectfully submitted that claim 16 is allowable and indication of such allowance is earnestly requested.

Claims 18-20:

Claims 18-20 are amended to depend on and further limit claim 16. Since claim 16 is believed allowable for the above reasons, claims 18-20 are also believed allowable for at least the same reasons as claim 16.

Claim 17:

Claim 17 is amended herein to explicitly claim all the limitations of claim 15, which were previously incorporated by reference. Thus, the amendment to claim 17 does not change the scope of the claim. Furthermore, amendment of claim 17 is not made to overcome the cited documents or for reasons of patentability.

Claim 17 recites, in part, "a plurality of multipliers, each of which includes an adder connected between an AND calculator and an output side XOR calculator." It is respectfully submitted that Riggle does not teach or suggest such claim limitations.

Turning to the specific citations of Riggle in the Office Action, Fig. 3 illustrates a flow chart of the decoding process performed by a syndrome computer, the error locator NU(X) and error evaluator W(x) computer, and the factor NU(x), evaluate W(x), and correction vector YI computer circuits of an integrated circuit. Riggle, col. 4, lines 28-32. In this figure, there is no structural detail regarding the circuit components. Therefore, Fig. 3 does not teach or suggest the limitations of claim 17.

Fig. 4 includes circuit details for computing syndromes simultaneously. Riggle, col. 11, lines 8-10. Nevertheless, the circuit of Fig. 4 shows a conventional AND-XOR structure, rather than the XOR-Adder-AND multiplier structure as recited in claim 17 of the present Application. Riggle, col. 11, lines 19-25 and Fig. 4. Similarly, Figs. 10, 13 and 23 do not teach or suggest the XOR-Adder-AND multiplier structure as recited in claim 17 of the present Application.

Column 11, lines 8-25 of Riggle describe the circuit depicted in Fig. 4. Riggle, col. 11, lines 8-10. It is respectfully submitted that this cited portion of the Riggle patent describes a conventional AND-XOR structure for realizing the multiplication function. Riggle, col. 11, lines 19-25. However, there is no mention of the XOR-Adder-AND multiplier structure as recited in claim 17 of the present Application.

Column 15, lines 15-23 of Riggle describe the circuit depicted in Fig. 10, stating, "Circuit 448 of FIG. 10 includes means for calculating error evaluator polynomial W(x). As embodied herein, the means for computing the values of error evaluator polynomial W(x) comprises w registers 450, amend syndrome 54 registers 210, error locator polynomial NV registers 352, multiplier 350, and treed adder 354 which executes the procedure shown in FIG. 3, including, specifically step 106." Riggle, col. 15, lines 15-23. It is respectfully submitted that this cited text in Riggle does not describe or suggest a XOR-Adder-AND multiplier structure as recited in claim 17 of the present Application.

Similarly, it is respectfully submitted that column 21, line 34 to column 22, line 5 of Riggle does not teach or suggest a XOR-Adder-AND multiplier structure as recited in claim 17 of the present Application.

For at least these reasons, claim 17 is not believed to be anticipated by Riggle. Moreover, it is respectfully submitted that claim 17 is allowable and indication of such allowance is earnestly requested.

CONCLUSION

In view of the forgoing remarks, it is respectfully submitted that this case is now in condition for allowance and such action is respectfully requested. If any points remain at issue that the Examiner feels could best be resolved by a telephone interview, the Examiner is urged to contact the attorney below.

Please change Deposit Account 50-0510 the $200 fee for an additional independent claim. No other fee is believed due with this Amendment, however, should such a fee be required please charge Deposit Account 50-0510. Should any extensions of time be required, please consider this a petition thereof and charge Deposit Account 50-0510 the required fee.

Respectfully submitted,

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